

PowerPC® 405 Embedded Cores

Reusable processor cores for high performance system-on-a-chip applications

Highlights

Compatible with the scalable and flexible PowerPC instruction set architecture to facilitate code reuse

Optimized for high performance, low cost, and low power consumption system-on-a-chip (SOC) designs

Supports product differentiation via inclusion of custom logic and/or low cost

JTAG and Trace FIFO ports enable robust debug capabilities, even in complex SOC designs

Available in the IBM Blue Logic™ core library for integration with peripheral and application-specific macro cores to develop SOC solutions

Supported by over 75 third-party vendors in IBM's PowerPC Embedded Tools™ Program

Full-function simulation models are available to support SWIFT compliant VHDL and Verilog simulation environments

PowerPC 405 CPU

- Compatible with PowerPC User Instruction Set Architecture
- Five-stage pipeline
- 32-bit x 32 general purpose registers
- Hardware multiply and divide
- Branch prediction

Cache Controllers

- Separate I- and D- cache units
- Fill-first, data forwarding
- Non-blocking flush operations
- Programmable loads and store

Memory Management Unit

- Variable page sizes (1 KB-16 MB)
- 64-entry fully-associative TLB

I/O Interfaces

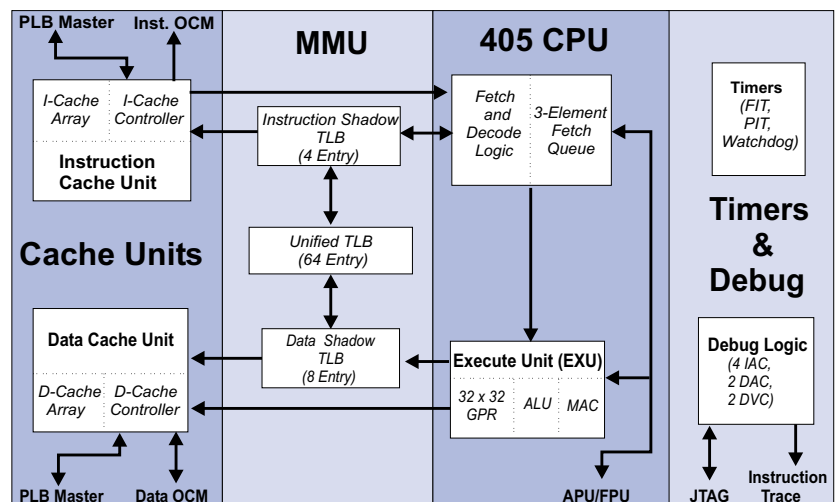
- Processor Local Bus (PLB)
- Auxiliary Processing Unit (APU)
- On-Chip Memory (OCM)
- JTAG

Timers

- 64-bit time-base
- Programmable interval timer
- Fixed interval timer
- Watchdog timer

Debug Support

- 4 Instruction Address, 2 Data Address, and 2 Data Value breakpoints
- Real-time non-invasive trace
- Exclusive traceback capability



PowerPC 405xx Core block diagram



Specifications	405A3	405B3	405D4
Technology	.25 μ m (.18 μ m L _{eff}) CMOS SA-12E	.25 μ m (.18 μ m L _{eff}) CMOS SA-12E	.18 μ m (.11 μ m L _{eff}) CMOS SA-27E
CPU Core Size (est.)	2mm ²	2mm ²	1.4mm ²
Frequency (MHz)	0 to 200 ^{WC1} 0 to 300 ^{TC1}	0 to 200 ^{WC1} 0 to 300 ^{TC1}	0 to 266 ^{WC2} 0 to 390 ^{TC2}
Performance (Dhrystone 2.1 MIPS)	282 @ 200MHz 423 @ 300MHz	282 @ 200MHz 423 @ 300MHz	375 @ 266MHz 550 @ 390MHz
Power Dissipation (estimated, typical)	1.0W @200MHz	650mW @200MHz	500mW @266MHz
Voltage	2.5V +/- 5%	2.5V +/- 5%	1.8V +/- 5%
I-Cache	32K	16K	16K
D-Cache	32K	8K	16K
MMU	Yes	Yes	Yes
Timers	Yes	Yes	Yes
JTAG	Yes	Yes	Yes
Trace FIFO	Yes	Yes	Yes

^{WC1}Worst case conditions (23V, 85° C, slow silicon) ^{TC1}Typical conditions (2.5V, 55° C, nominal silicon)

^{WC2}Worst case conditions (1.65V, 85° C, slow silicon) ^{TC2}Typical conditions (1.8V, 55° C, nominal silicon)

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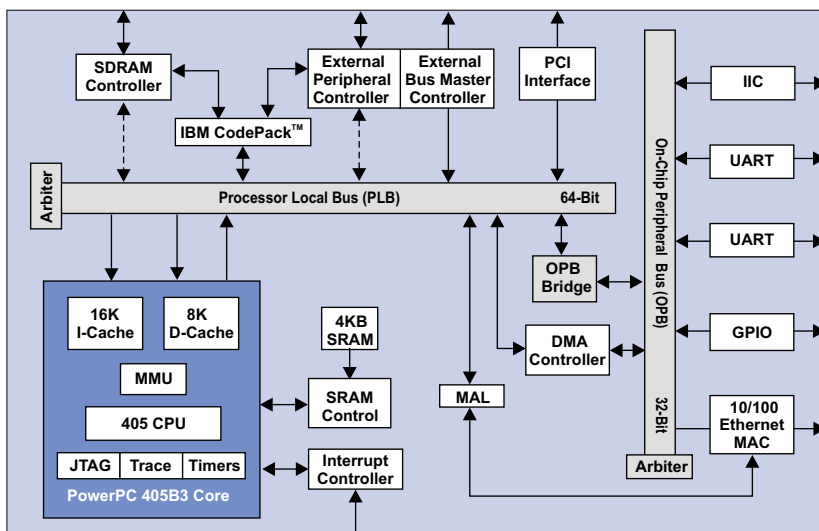
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PowerPC 405 Core Integration

Through the IBM CoreConnect™ bus architecture, PowerPC 405 cores integrate on-chip with and other reusable peripheral and application-specific cores, such as the controllers and CodePack™ code decompression shown in the example below. High speed, high bandwidth peripherals, like the 405 core, directly attach to the processor local bus (PLB). Less performance-critical cores attach to the on-chip peripheral bus (OPB).

The PowerPC 405 cores and the CoreConnect bus are available through the Blue Logic core library to help reduce time to market of SOC designs.

For more information on IBM Microelectronics core offerings, view the Blue Logic core library at www.chips.ibm.com/products/asics/ or contact your local IBM Microelectronics sales office.



IBM PowerPC 405GP embedded processor showing integration of 405B3 core



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